

11002 U.S. PTO
10/032646

12/27/01

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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

364-905

APPL NUM 10032646	FILING DATE 12/27/2001	CLASS 257	SUBCLASS 374	GAU 2811	EXAMINER Loke
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**APPLICANTS: Randolph Mark;

**CONTINUING DATA VERIFIED:

none.
Loke

** FOREIGN APPLICATIONS VERIFIED:

none
Loke

PG-PUB	DO NOT PUBLISH <input checked="" type="checkbox"/>	RESCIND <input type="checkbox"/>	
Foreign priority claimed	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	ATTORNEY DOCKET NO	
35 USC 119 conditions met	<input type="checkbox"/> yes <input checked="" type="checkbox"/> no	G0727/2243P	
Verified and Acknowledged Examiners's initials Loke			

TITLE : Planar transistor structure using isolation implants for improved Vss resistance and for process simplification

U.S. DEPT. OF COM. / PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs. Drwg.
		Print Fig.	
<input type="checkbox"/> TERMINAL DISCLAIMER		Application Examiner	
		PREPARED FOR ISSUE	
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